MULTIPLE MIRROR TELESCOPE OBSERVATORY

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Internal Technical Memorandum 87-3
Subject: MMTO Reticon System
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Introduction

This memorandum is prepared from notes taken during a three-day in-house tutorial presented by Dr. John Geary of SAO in October 1986. The function and some of the design considerations for the Reticon detector systems used on the MMT spectrograph and the Echelle spectrograph are described. A system consists of four major areas: the "Head" and the "mother" box which reside on the instrument, and the Discriminator chassis and computer I/O which reside in the computer room.

Recommendations for improvements are listed at the close of the document.

The "Head"

The Head consists of dual linear array Reticon^{tm} detectors and two circuit boards that contain the clock drivers, voltage references, reset and start circuitry, the four signal preamps and clamping circuitry. There are two separate Reticon chips in the Echelle spectrograph, whereas both arrays are on the same chip in the case of the MMT spectrograph. The two Echelle Reticon chips are interfaced to an intensifier package by a split fiber optic boule. The single MMT spectrograph Reticon chip is similarly interfaced.

The "mother" box (to be discussed in detail later) provides all the necessary clock, reset and start signals, as well as the power to the Head.

The Reticon

The Reticon is a linear photodiode array of either 1024 diodes or 936 diodes. Both are driven the same by the SAO electronics; the electronics for the 936 just scan past the array and assume 88 dummy diodes. The linear array is sub-divided into odd and even diodes; odd diodes are numbered starting at 1 and even starting at 2. Each diode is connected to an MOS switch which in turn is connected to one of two common video lines. All the odd diodes are connected to the "odd video" line and all the even diodes connected to the "even video" line. Odd and even diodes are read simultaneously. To read the diodes, a logic "1" is propagated along the array by the internal shift register, driven by a complementary pair of clock transitions.

The dual detector arrangement is called out as "A" video being the left Reticon and "B" the right. Both Reticon arrays are read out at the same time, with the Start, Reset and Clock signals wired in parallel to each. Thus there are four video outputs total and one can see four BNC bulkheads on the Head labeled "A odd," "A even," "B odd," and "B even."

Sampling

The array readout is started by a low level "Start" pulse, shown as "$\overline{S}$" on the timing diagram in Figure 1. A "1" is loaded into the Reticon shift registers on a rising edge of the 500 kHz clock signal "ϕ1", switching the first diodes on to the video lines. The "Reset" pulse then grounds the video lines to back-bias the diodes that are currently switched onto the video lines. (Note a change to discussing the diodes in singular to simplify the wording, remembering that there are four diodes all being read at one time.) A back-bias voltage of 5.15 vdc is developed across the diode at Reset. The back-biased diode is then isolated from the video line when the next diode is switched onto the video line. The freshly reset, isolated diode then acts like a photoconductive capacitive element and the anode charges up as a function of the intensity of the light to which the diode is exposed. The anode of the diode will charge to a full voltage of 5 vdc and be saturated if overexposed. The voltage on the diode's anode becomes the video signal when the diode is read out. A diode read (shift) occurs on each ϕ1 clock transition after the start pulse has been received.

For true correlated sampling, it would be necessary to read a diode, switch the diode off-line and Reset it, then read the next diode. The Reticon, however, is wired so that Reset must be done with the diode on the video line. Thus the video signal is developed by finding the difference between the voltage level on the freshly reset diode "n" and the charged diode "n + 1." Such sampling is termed quasi-correlated double sampling.

There is no diode on the line before the "Start" pulse so that the difference taken for the first diode is different from the others. The difference in this special case is the value of the video line before the first diode is on the line subtracted from the value of the line with the first diode on the line. The first diode may provide an anomalous signal as a result but still provides useful video.

Drivers and V_{bias} (Board #1 of the Head Electronics)

The complementary clock lines need high power drivers because of the capacitance on the Reticon shift registers. MH0026 drivers were used in this design. The clock drivers on the Echelle Reticon are mounted on the back of the mounting flange because of initial concern about temperature drift. The clock drivers on card 1 are not used in this case.

Tests showed that an external transistor to drive "Reset" caused less noise than the Reset transistor on board the Reticon chip; however, the temperature of the external transistor must track the detector temperature well or the baseline (to be explained later) will vary. There is an external "Reset" transistor for each video line (4 total). The transistors are driven by a 4049 MOS driver where -8 v is off and +5 v is on.

The voltage used for back-biasing the diodes during Reset, V_{bias}, is generated by an LM356 from VREF (from board 2). Bias passes through a low pass filter (100 ohm by 10 uf) into a FET op amp. The electrolytic capacitor was installed backwards early on and caused "bursting" of the video signal.

The Preamplifiers (Board #1 of the Head Electronics)

The preamplifier uses two FET's and two low noise bipolar transistors. The preamp must have high gain (+58) and a fast settling time and slew rate. The preamp dc offset is empirically trimmed so that the output of the preamp is near zero volts for zero illumination. There are four identical preamps,

one for each video line.

The two boards in the Head are connected by solid wires and resistors that connect around the periphery of the boards. This may not be the best for reliability and freedom of access, but it does permit access to the important signals for testing. The video preamp outputs appear on the 220 ohm resistors between the two cards.

Power (Board #2 of the Head Electronics)

Very stable and quiet voltages +V (5.15 vdc) and -V (-8.39 vdc) are generated from a pair of LM329 (6.95 v voltage references). VREF, used to generate V_{bias} as discussed earlier, is tapped from the +6.95 v reference and sent to board 1. A dual TL082 FET op amp is used to adjust and to regulate the +5.15 v and -8.39 v voltages which in turn are used to power the clock and Reset drivers. Filter capacitors on the op amps have long time-constants which cause a noticeable delay in the time to stabilize when power is first turned on. The same scheme is used in Geary's new CCD to get very quiet power supplies.

Clock, Reset and Start Timing Signals (Board #2 of the Head Electronics)

The 500 kHz clock signals are received differentially from the "mother" box. The required complementary clock for the Reticon chips is then re-generated and passed to board 1.

The start and reset pulses are received single-ended, buffered and then sent to board 1.

Video Clamping/Sampling (Board #2 of Head Electronics)

The clamp command pulse is received differentially from the "mother" box and a single-ended signal sent to the clamp circuitry. The video from the preamps is AC-coupled immediately before the clamp circuit to remove any DC bias from the video signal. The clamp (to ground) reduces the amplitude of the reset transient spike and also reduces the dynamic range of the signal to ease the requirements on the next stage of amplification. Releasing the clamp from the AC-coupled video line results in analog subtraction (sampling). The sampled video signal is then amplified and output to the BNC connectors on the back of the Head assembly. The signal is transmitted to a second clamp/sampler in the "mother" box. The second clamp is not in the Head because there was not room. The video is biased slightly positive because the slew rate of the amplifier is not symmetrical and not as fast when biased negatively.

Ground reference is the Head chassis metal and goes back through the coax signal cables to the "mother" box.

The "Mother" Box

The "mother" box contains three circuit cards. One card is dedicated to generating the timing for the quasi-correlated double sampling. The other two cards are dual channel video analog-to-digital converter boards. Two identical boards are used, one for the left array and one for the right. The dual channel (odd/even) A/D boards contain receiver amplifiers, the second stage clamp/sampler, dynamic offset circuitry and a digital multiplexer to combine the odd and even video from a single array into a single 1024 1 MHz 8-bit parallel data stream. The two (left/right) 1024 8-bit parallel data streams

are then sent to the Discriminator chassis for further processing.

Timing Board

An 8 MHz clock is used to clock a modulo 16 counter and provides 16 counts per diode read; the timings of some of the major signals are as shown in Figure 1. Within a given video line (odd and even) another sub-division is defined that may be somewhat confusing. The odd and even video lines are further subdivided into odd and even elements (see Figure 1 $\overline{O}/E$ line) giving odd-odd and odd-even elements. Likewise, the even video line produces even-odd and even-even elements.

Video A/D Board

The video signals are received at the "mother" box by two LM318's located on the A/D board. LM318's are slightly unstable at unity gain without a feedback resistor, but this instability does not appear to produce any problems. Adding a feedback resistor would slow the 318 down a little. A better solution would be to replace the 318's with LH0002's and should be considered.

The second stage clamp and sampler perform an analog subtraction of the video at count 7 from whatever it's doing at count 8. The video at count 7 is the running baseline which should have settled to a stable value following Reset. The settling to a stable value allows the video signal to be dynamically referenced to ground using the subtraction technique. A stable level (at count 7) prior to video level is the requirement for good video.

Fixed Pattern Noise

Every other diode on each video line has a different DC reference; i.e., the average offset of the even diodes is not equal to the average offset of the odd diodes. Two adjustable voltages are dynamically switched using DG303 MOS switches to subtract out the average offset for all the odd-odd and even-odd diodes, and two different voltages are similarly switched in for all the odd-even and even-even diodes. This dynamic offset must be provided; otherwise, the range of the offsets could exceed the dynamic range of the ADC. There are (4) potentiometers located on the card edges of each of the ADC boards for use in adjusting the offsets.

The effect of varying offset produces what is called "fixed pattern" noise and is caused by feed-through in the Reticon chip from clock signals. This feed-through varies from element to element. Note the offsets are entirely in the Reticon; the electronics are stable and do not contribute.

There remains a residual fixed pattern that changes with temperature. It is wise to trim the offsets, using the (4) potentiometers, each time the instrument is set up on the telescope, after the detector has cooled down to operating temperature. The offsets are trimmed using the alignment tool. Do not set the offset to zero; a slight positive offset minimizes the effect of drift and ensures that the video remains on scale for the ADC. Any signal falling below zero will be clipped to zero; i.e., the "no light level" should be slightly positive. Also, we do not want the signal to saturate; doing so will result in unstable centroiding, explained in the Discriminator section. Saturation is prevented by setting the image intensifier gain to a level where few or none of the photo-electron events saturate the range of the ADC, as seen on the output video of the alignment tool. Typical average pulse heights under these conditions are approximately 4 volts out of a full scale of 10 volts.

With a much smarter controller, the offsets for each individual diode could be subtracted out with a lookup table having separate values for each element. Variations with temperature could be sensed and the lookup table updated accordingly, provided that variations with temperature are repeatable.

Analog to Digital Conversion

The ADC is a serial converter, not a flash ADC, so conversion time takes up most of the following read cycle. The conversion is done in about 1/2 a diode time. Sample and hold amplifiers are used to hold the video stable while the A/D conversion is taking place. The TDC 1001J is an 8 bit ADC, is monotonic and was the best converter available at the time that would fit on the board. A resistive divider before the ADC ensures limiting the signal to the range of the converter, 0 to 0.5 vdc. The resistor divider also reduces the effect of the capacitance intrinsic to the input of the ADC. Each ADC provides 512 8-bit words per line.

The design uses two ADC's, one for each video signal because the converters were not that expensive and they save multiplexing the video to a single device. Combining of the odd and even video signals for each of the two Reticon arrays is done with a digital multiplexer following the ADC, giving two 8-bit parallel data paths operating at a 1 MHz word rate, each transmitting 1024 words per frame.

Fliers

A flier is an anomalous event such as an ion event which causes occasional saturation over a few pixels. It can also be a "hot" diode which has an offset considerably different from the average. Centroiding in the Discriminator is skewed by saturated pulses; however, dark current of the image tube is the dominant dark count effect, not ion events. An ion event occurs every few seconds in normal operation. Frame-to-frame subtraction corrects for hot diodes simply by subtracting them out, since the anomalous value repeats in subsequent frames.

Signal Cable to Discriminator

Optocouplers and differential drivers, also located on the A/D boards, are used to transmit signals to the Discriminator. The cable for these signals needs a minimum of nineteen twisted pairs: eight per video channel, one for reference ground (for optoisolator) plus two for the clock and sync signals. The 3486 differential driver is preferred for such an application now, but that chip was not available when the system was first designed. Higher powered terminating resistors (330/390) would be better for noise immunity than those in use, but the drivers currently in use can not handle this high a load.

Problems with crosstalk between the "sync" and "clock" signals lead us to ground the "sync" line for "B" and the "clock" line for "A," so as to provide better shielding between the single sync and clock signals in the ribbon cable. Replacing the cable with individually shielded twisted pairs and improving the drivers and the noise immunity would help ensure that these signals are received cleanly.

Timing to Discriminator

The 16 MHz clock is divided down to 8 MHz because the optoisolator for this design can't handle 16 MHz. This 8 MHz clock serves as a master clock for the Discriminator chassis.

We could use "S" to synchronize the Discriminator chassis, but we use "Sync" instead. Sync is delayed eight pixel intervals to compensate for the delay introduced by the smoothing function in the Discriminator and is approximately equal to the width of this smoothing function. The delay allows the first pixel event to occur at the beginning of the active address time in the Discriminator. The time delay is developed in the "mother" box because there is more room there.

The Alignment Tool

An alignment tool contains two DAC's to reconvert the 8-bit video to analog in the same way as in the Discriminator chassis. To use the tool, the cables to the Discriminator must be disconnected and the alignment tool cables connected. Adjustment of the four offset trim pots to minimize the fixed pattern noise can easily be done when the spectrograph is mounted on the telescope. The DAC provides a voltage swing of 0 - 10 vdc full scale. The trim offsets should be set for approximately 10% of full scale and equal in each channel. Synchronization and data latching are accomplished in the same way as in the Discriminator chassis. The alignment tool is also helpful in troubleshooting the "mother" box.

Troubleshooting the Head and "Mother" Box

First look at the video coming out of the Head and check the cables and connectors. A bad cable or loose connection are the two most common problems. Wiggling the coaxial cables used for the video signals may cause the problem to come and go, for example. If the video coming out is bad or there is no video at all, the signals to the Head should be checked.

Check the signals and power on the cable from the "mother" box to the Head with an oscilloscope. Power to the Head as well as the clock and timing signals are routed through a 25-pin D connector. A problem here can cause the entire operation to look very bad.

If all the signals and power to the Head look good and the video from the Head is still bad, then it may be time to open the Head up. This is not a simple procedure and will result in at least a half a night/day of downtime and possible wavelength shifts.

First the Head must be removed from the spectrograph. Removing the Head from a cold tube is tricky and delicate and should be done with the utmost caution and only when absolutely necessary.

Inspect the connections between the circuit boards and the Reticon chips and the connections to the four coax connectors. They have previously been found broken. The back plate of the Head is spring-mounted and the flexure can result in broken connections.

If all is OK, then inspect the signal board inter-connections around the periphery of the Head electronics. Checking components on the Head circuit boards must be done with extreme care.

Occasional problems have occurred with the differential drivers in the system used on the ridge, apparently from lightning, but not at the MMT.

No problem has ever occurred with the active components of the preamplifier in the field.

The Discriminator

The Discriminator is a multicard chassis that resides in the equipment bay next to the Point 4 instrument computer in the computer room. There are two chassis, one for the Echelle Reticon and one for the MMT spectrograph Reticon. The only difference may be some matching to the image tube on the filter board used to perform the smoothing function. The Discriminator converts the digital video signals from the "mother" box to analog, performs a centroiding and smoothing operation, and presents the resulting event count as a series of addresses to the computer interface. The Discriminator chassis uses DGC bit nomenclature for the centroided event addresses, where MSB = bit 0, LSB = bit 15.

Note on edge connector numbering: some drawings are shown with connectors numbered 1 - 72, others 1 - 36 double-sided.

Card 5: Receiver and Output Drivers

The differential receivers used to receive signals from the "mother" box are 8820's. B_{clock} and A_{sync} are received along with two parallel 8-bit video data lines. A_{clock} and B_{sync} are tied to ground to reduce crosstalk in the cable. A 100 pf capacitor on the clock signal prevents spurious signals but reduces the bandwidth. The differential receivers could stand to be updated.

"Simulator Enable" is a signal that comes from the simulator enable switch mounted on a panel at the back of the chassis. This function generates a simulated photon signal for a test consisting of a "picket fence" profile of "boxcar" or single element pulses. The test signal is imposed on every 4 to 16 frames; the function can't generate pulses every frame or they will be subtracted out. The simulation is used to check operation of the smoothing function in the Discriminator.

Gates on card 5 permit selection of data or simulator. The simulator itself is on card 3.

Diode arrays for protection are shown on the schematic but have been removed. We have had no problem with failures as a result of transients on the transmission lines.

Card 3: Address Timing Generator and Simulator

The "sync" pulse starts a counter. The counter provides running addresses, four per physical diode, by dividing down 8 MHz. EA12 to EA00 is the address space, but EA12 is not used. EA12 was originally provided for odd/even framing which is not used so that the actual address space sent to the interface board is EA11 to EA00. This provides 4096 bins for the 1024 pixels, or 1/4 diode binning.

The backplane is a problem for the timing signals; 8 MHz is too fast for the handwired bus and driving clock inputs on lots of little bitty boards. To compensate, there is only one clock receiver per board; the receiver then provides the required number of clock inputs for that board.

The point spread function of the image tube limits the resolution. An improvement from 1/2 diode binning to 1/4 diode binning improves the resolution from 30 microns to 20 microns, not 15 microns. Greater resolution in binning would improve the resolution by only a few microns because the limit imposed by the image tube is being asymptotically approached. The achieved resolution is also limited by magnetic and mechanical flexure of the tube and by the finite slit width that must be used.

The simulator: Banks of switches give two 8-bit words which go to latches. Jumpers on B7 select the frame interval between the frames containing simulated data. Choices are every other frame, every four frames, every eight, and every sixteen. The Simulator Enable switch is on the back of the chassis. "Simulator Enable" is indicated on the front of the chassis with an LED.

A preset counter on this card generates an enable that can shift the perceived centroid of the simulated data. One can skew the smoothed pulse by changing switches. This feature is not used.

The simulator has its own 16 MHz oscillator and sync generator. A 1 of 8 decoder provides strobes to time out things like read-subtract-memory, setup-time-for-the-memory-read, latch-the-result, do-comparisons, write-back-to-the-frame-memory, and strobe-out-the-digital-result-to-go-to-the-analog-centroid.

Card 7 and 9: Frame Subtract

Frame subtraction is necessary so that photo-electron pulses are counted only once. Without such frame subtraction, the long phosphor decay times would result in multiple counting. Circuitry on this card stores every incoming frame and subtracts it from the next frame. The memory used is 1k by 8 RAM (2114's). The subtracted value goes on to the next card to be centroided. When we do the subtraction, we actually do the addition of a complement with an end-around carry. If subtraction results in a negative number as detected by the state of the carry, the result is forced to zero.

"DX Data" stands for "DA Data" or "DB Data." The data frame is stored in two different places, one for "subtract" and one for "compare less than previous." If the current frame value for any one diode is less than the previous value for the same diode, then the DX output is forced to zero for that diode to prevent double-counting.

A switch on the back panel permits transmitting raw data for test. Raw data will give spurious results on the computer output; it is used only for checking the circuit up to frame subtract. No status signal is provided to the computer to indicate that the Discriminator is in the test mode; it would be desirable, though the absence of such a signal has not been a problem.

Card 11 and 13: DAC and Event Detection

The subtracted video is converted to analog for the next operation. A smoothing function is performed by two 2-pole filters. The pulses should look quasi-Gaussian, so symmetrical smoothing must be avoided. A long "tail" on the output, especially a negative tail, was also unacceptable. The filter design to do this is a result of a lot of empirical fiddling. There may be two different filters, one for Big Blue and one for the Varo. These are different because the point spread functions of the image tubes are different. The filter is optimized for the image tube used with that Discriminator chassis; otherwise, the chassis should be interchangeable. In changing from one Varo image tube to another, the filter stays the same. But if the image tube type is changed, the filter may require adjustment. The Varo image tube gives out broader pulses than Big Blue, for example. Poor optical contact of the Reticon with the image tube will mess up smoothing, producing pulses wider than usual.

The DAC is the AD561, same as in the alignment tool. It is a 10-bit DAC, but only the eight upper bits are used. The two LSB's are tied to ground. A precision voltage output (+5 v) goes to the potentiometer on the front panel, then through a filter to one leg of a Discriminator (LM319). Analog video

goes to the other leg. The video is trimmed to maintain a bias on the signal. Unsmoothed video goes to a BNC on the back panel for test. Smoothed video also goes to a BNC for test.

The analog video signal goes to two places. One is the upper half of the LM319 dual high speed Discriminator which is used as an event window Discriminator. The quasi-Guassian input results in a pulse output whose width is a function of the Discriminator setting. Diodes clamp the Discriminator input at 0.6 v for protection. The Discriminator pulse output goes to a shift register which synchronizes the pulse with the 8 MHz. Edges of the pulse start out asynchronous but end up synchronous. This pulse is now called the "event window."

The second place the analog video goes is to a differentiator. The resulting pulse is fed to the other half of the Discriminator. The differentiated pulse must rise to the threshold of the Discriminator during the event window time to produce a recorded event. The effect is to discriminate against noise and small pulses which do not represent true photo-electron events on the image tube. The actual address of an event occurs when a zero-crossing of the differentiated signal occurs within an event window. This address is sent to the computer interface board. The interface board will do a "read modify write" to that address to add 1 count to that bin.

Card 15: SE/PE (Simultaneous Event/Previous Event Logic Board)

As discussed under Frame Subtraction, every effort must be made to prevent recording multiple counts from a single event in order to ensure the integrity of the data. Even with frame subtraction, it is possible to count a single event twice, depending on the exact timing relationships between the events and the frame time. Board 15 provides veto power to prevent just such double counting. Basically, if a pulse occurs at the same pixel as a pulse on the previous frame, it is assumed that the first sampling occurred on the rising slope of the photo-electron event, and a second count at this address should be suppressed. A memory keeps track of the previous frame for this purpose. A one frame veto is sufficient because the rise time of the scintillation is about ten times faster than the frame rate.

There is also a circuit to veto any event that occurs simultaneously on the same diode on the two adjacent Reticon arrays. An event on the interface of the split fiber optic boule would cause the event to be counted on both arrays. For the boules currently in use, this doesn't happen, so this circuit is disabled.

Two 2102 RAM's (1k x 1) keep track of previous events. These memories do not record data values; they store only a flag for each diode where an event occurred during that frame.

Centroiding is not perfect to the 1/4 diode level, maybe to the 1/2 diode level. We veto a band of diodes for this reason because of inexact centroiding. The band is four diodes.

The dead time imposed by the veto circuitry is 1 ms (i.e., one frame time) after a perceived event. A light level causing photoelectron events to arrive at intervals approaching 1 msec will cause "pile-up" and pile-up causes errors, so the maximum count rate turns out to be 3000 - 4000 counts/sec/array. It really doesn't necessarily bother the Varo image tube to handle 10,000 counts per second, but the counting efficiency and centroiding will be compromised. Close pulses, for instance, would be resolved as single pulses but with incorrect centroids.

Signals to the Computer Interface Board

Running addresses are returned to card #5 where the drivers transmit the information to the computer interface. A_{data} and B_{data} strobes derived from the windowing functions described above strobe the addresses from arrays A and B into the interface board.

Computer Interface Board

The computer interface board is used with either the Echelle spectrograph Discriminator or the MMT spectrograph Discriminator. The circuit was designed and built in-house on a large scale DGC "Nova" interface board. The board accumulates the event count for each "bin" of the Reticon array by performing a read, add +1, write-back to the addresses transmitted by the Discriminator chassis. The bins are reset and read out under programmed I/O control from the Point 4 computer. The board resides in the first expansion chassis on the Instrument computer.

At the time the board was designed, it was necessary to use relatively small memory chips. Thirty-two memory chips were required for the two 4k x 16 memory buffers for the two arrays. Space requirements prevented the use of the standard "4040" board, so it was necessary to provide all the bus housekeeping circuits to interface with the DGC bus. The memory chips used are 4104 static RAM's. Accumulate and "stop integration" control are received from the computer. The I/O board includes a 5 MHz oscillator to clock the memory.

Data are fed to the computer via PIO; no DMA is provided. The PIO is interrupt driven. There is no handshake with the Discriminator chassis; it hasn't been necessary.

A test mode permits writing a known pattern to a latch on the interface board and reading it back to check out operation of the interface board and memory.

Overload and Discriminator Panel Readings

The count display on the operator's console, the display on the Discriminator chassis, and the display on the Lexiscope monitor are computed a different way and agree only to about 7%. Separate displays are safety valves to permit shutting down in the event of overexposure. A computer independent emergency shutdown is necessary to ensure the image tube is protected. The front stage of Big Blue is irreplaceable. Shutdown occurs now as a result of array overillumination (overall count rate too high) or saturation (no count rate).

We could have an alarm for overload of individual diodes. The problem here is differentiating between a dangerous saturation condition and an ion event. We would need an override or logic and timing to prevent erroneous shutdown. Perhaps a circuit could be devised which would cause overload shutdown if more than n pixels in m frames were overloaded.

Things to do:

The existing flat red and white twisted pair cable (Peppermint Patty) should be replaced with individually shielded twisted pair cabling.

The count overload configuration should be cleaned up, documented, and possibly improved.

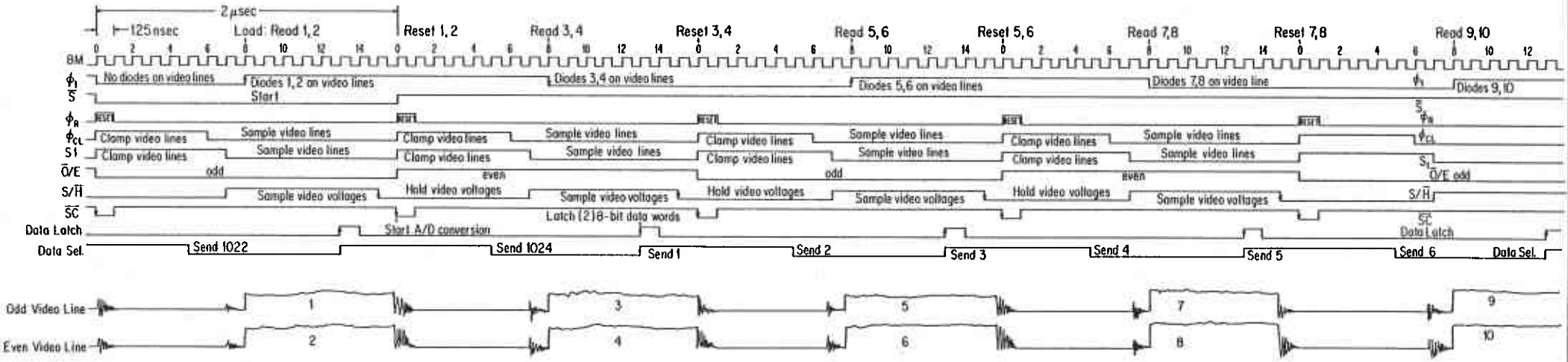
A spare computer I/O board should be built.

Beefed-up line drivers for the video to the "mother" box should be considered to improve the quality of the baseline.

The -15 VDC supply has failed twice. A replacement should be considered. A linear power supply is preferable. The supply should be located next to the Head to reduce noise pickup. The resulting space limitations may preclude overvoltage protection but such protection is desirable, if possible. A supply did fail high once, doing considerable damage to the electronics.

Improved differential line drivers and receivers for signals to the Discriminator chassis should be considered.

Some repackaging of the "mother" box for reliability and to reduce RFI may be indicated.


2 μsec
125 nsec
Load: Read 1, 2
Reset 1, 2
Read 3, 4
Reset 3, 4
Read 5, 6
Reset 5, 6
Read 7, 8
Reset 7, 8
Read 9, 10
BM
No diodes on video lines
Diodes 1, 2 on video lines
Diodes 3, 4 on video lines
Diodes 5, 6 on video lines
Diodes 7, 8 on video line
Diodes 9, 10
Start
Clamp video lines
Sample video lines
Clamp video lines
Sample video lines
Clamp video lines
Sample video lines
Clamp video lines
Sample video lines
Clamp video lines
Sample video lines
Clamp video lines
Sample video lines
odd
even
odd
even
odd
Sample video voltages
Hold video voltages
Sample video voltages
Hold video voltages
Sample video voltages
Hold video voltages
Sample video voltages
Hold video voltages
Sample video voltages
Latch (2) 8-bit data words
Start A/D conversion
Send 1022
Send 1024
Send 1
Send 2
Send 3
Send 4
Send 5
Send 6
Odd Video Line
Even Video Line
1
2
3
4
5
6
7
8
9
10